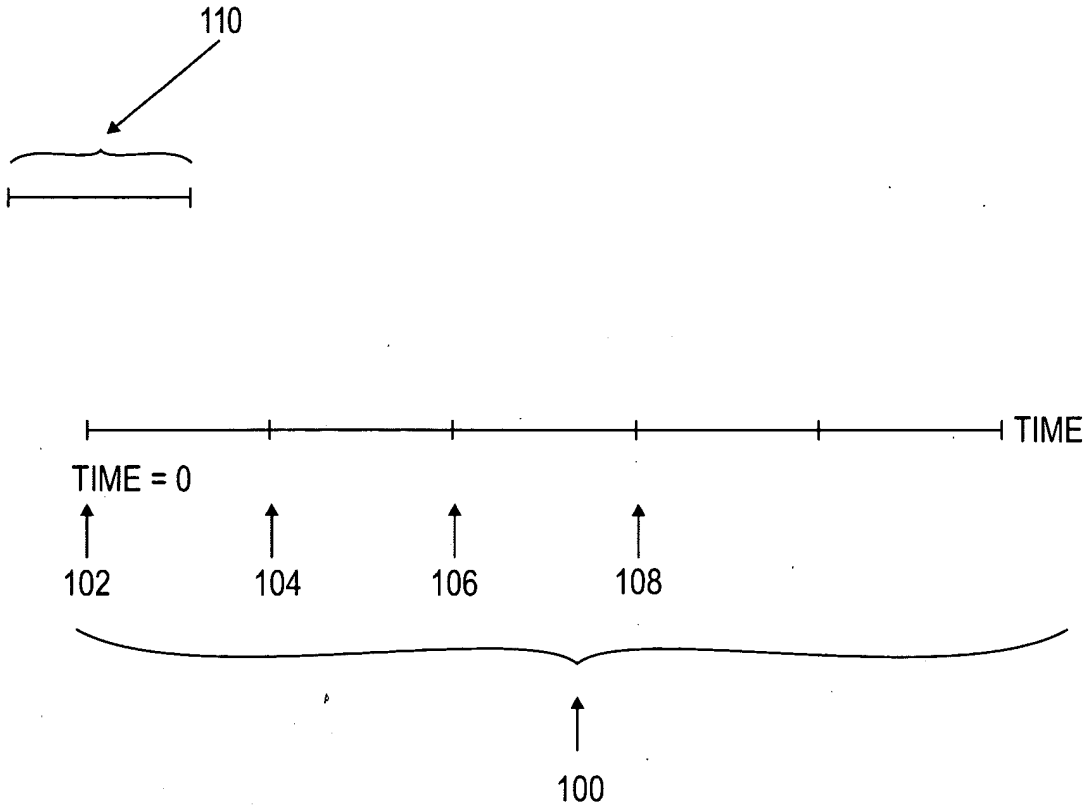


Fig. 1

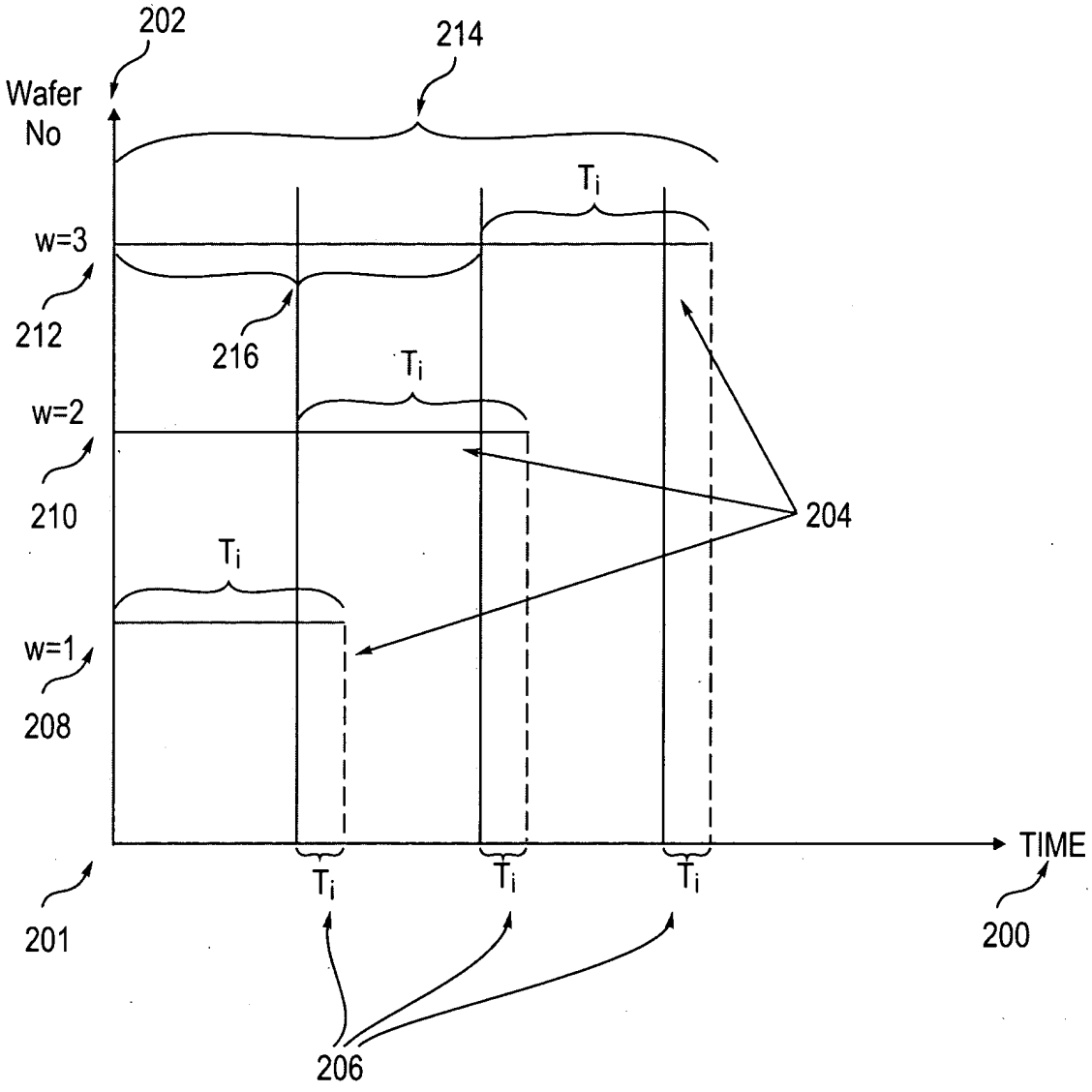

202
214
Wafer
No
T_i
w=3
212
216
T_i
w=2
210
204
T_i
w=1
208
TIME
T_i
T_i
T_i
201
200
206

Fig. 2

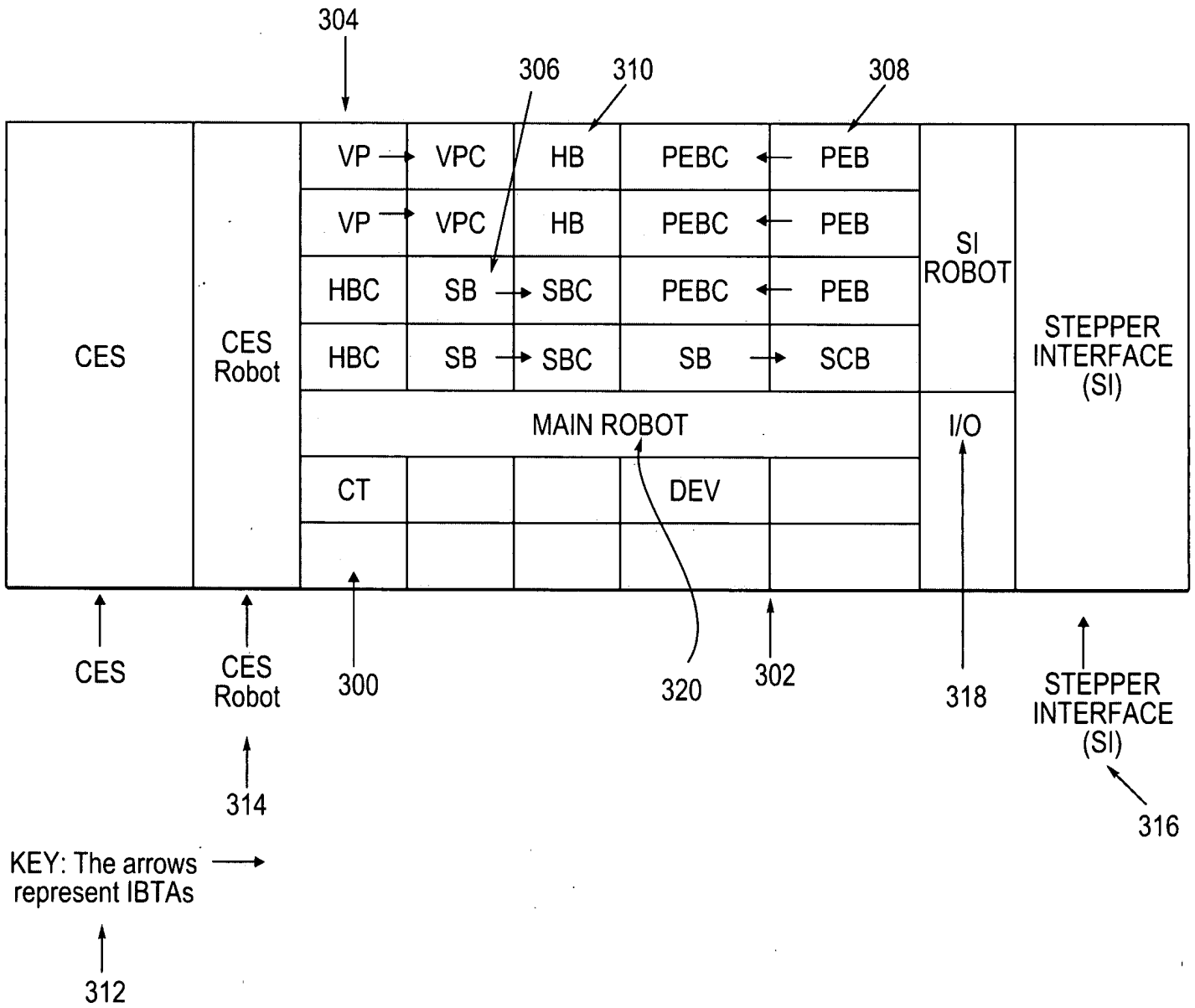
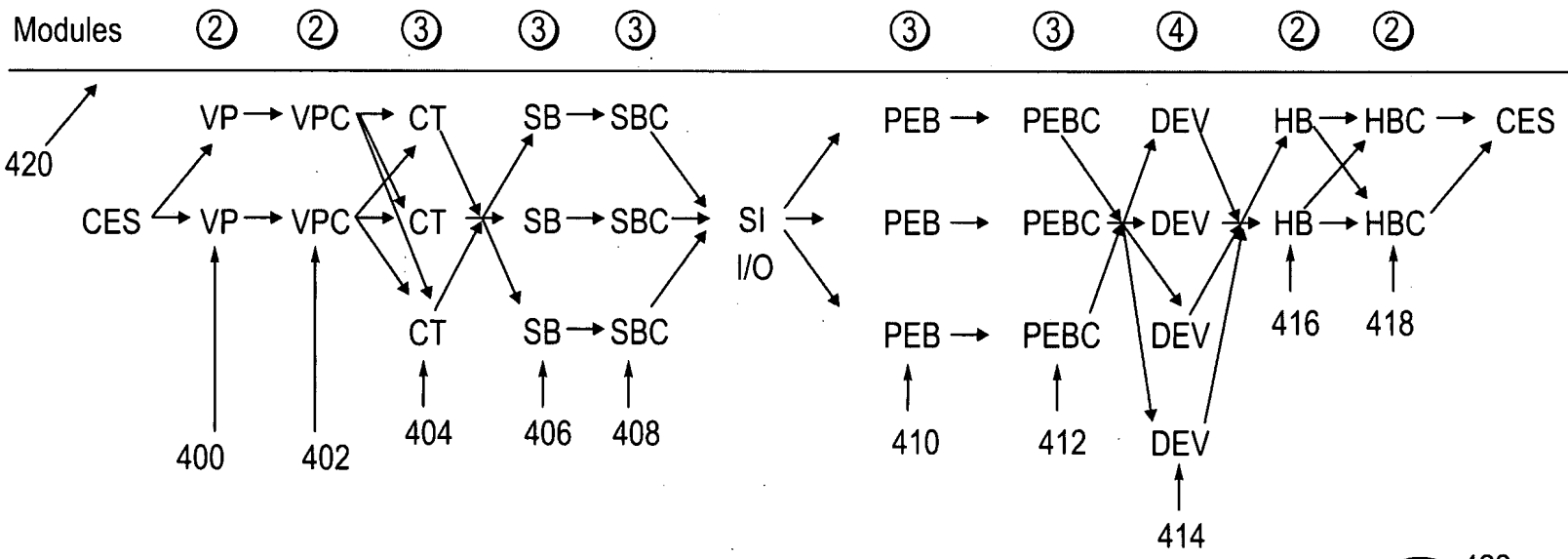

304
306
310
308
VP
VPC
HB
PEBC
PEB
VP
VPC
HB
PEBC
PEB
HBC
SB
SBC
PEBC
PEB
HBC
SB
SBC
SB
SCB
SI ROBOT
CES
CES Robot
MAIN ROBOT
I/O
STEPPER INTERFACE (SI)
CT
DEV
CES
CES Robot
300
320
302
318
STEPPER INTERFACE (SI)
314
316
KEY: The arrows represent IBTAs
312

Fig. 3



422

Module PATH	VP	VPC	CT	SB	SBC	PEB	PEBC	DEV	HB	HBC
1	1	1	1	1	1	1	1	1	1	1
2	2	2	2	2	2	2	2	2	2	2
3	1	1	3	3	3	3	3	3	1	1
4	2	2	1	1	1	1	1	4	2	2
5	1	1	2	2	2	2	2	1	1	1
6	2	2	3	3	3	3	3	2	2	2
7	1	1	1	1	1	1	1	3	1	1
8	2	2	2	2	2	2	2	4	2	2
9	1	1	3	3	3	3	3	1	1	1
10	2	2	1	1	1	1	1	2	2	2
11	1	1	2	2	2	2	2	3	1	1
12	2	2	3	3	3	3	3	4	2	2

Fig. 4

Module Type Type	Process Time	Overhead Time	Process + Overhead
VP	52	10	62
VPC	60	5	65
CT	46	10	56
SB	60	7	67
SBC	45	5	50
PEB	60	5	65
PEBC	45	5	50
DEV	100	10	110
HB	25	10	35
HBC	22	10	32
EXPOSURE	10	15	25
OEBR	20	5	25
TARC	60	10	70
BARC	60	6	66
More?			

Transport Type	Trnsport Time
CES	6
Captive-1	6
Captive-2	6
SI	6
IBTA	5
More?	

LOAD-LOCK = CASSETTE

System throughtout, (WPH) → 80
System takt time (sec/wafer) → 45

504 506 508

Process Step	Module type Transport used used	Process + Overhead Time	Transport Time	Module Takt Time	Number of Modules Required	Funda-mental Period
0	CASSETTE	0		0		
	CES		6			
1	VP	62		74	2	20.00
	IBTA		5			
2	VPC	65		75	2	38.00
	C-1		6			
3	CT	56		68	2	38.50
	C-1		6			
4	SB	67		79	2	38.50
	IBTA		5			
5	SBC	50		60	2	20.00
	C-1		5			
6	EXPOSURE	25		35	1	28.00
	S1		6			
7	PEB	65		77	2	34.25
	IBTA		5			
8	PEBC	50		60	2	37.50
	C-1		6			
9	DEV	110		122	3	35.00
	C-1		6			
10	HB	35		47	2	35.00
	C-1		6			
11	HBC	32		44	1	37.50
	CES		6			
12	CASSETTE	0		12	1	32.50
			0			
13	Vacant	0				
			0			
14	Vacant	0				
			0			
15	Vacant	0				
			0			
16	Vacant	0				
			0			
17	Vacant	0				
			0			
18	Vacant	0				
			0			
					22	38.5

500 502

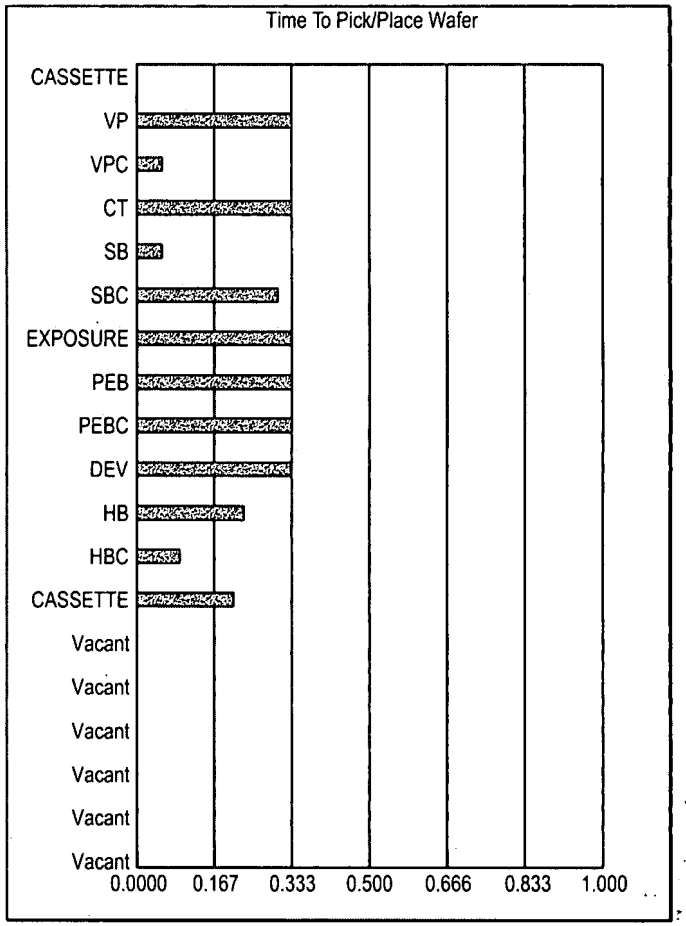
No. Of Modules →
Minimum sending rate → 45
Actual sending rate → 45

Fig. 5

Actual sending period →

Process Step	Module type Transport type	Process + Overhead Time	Transport Time	Time module need to be served		
				Actual	Ti Normalized	Normalized
0	CASSETTE	0		0	0.000	0.000
	CES		6			
1	VP	62		68	1.511	0.511
	IBTA		5			
2	VPC	65		138	3.067	0.067
	C-1		6			
3	CT	56		200	4.444	4.444
	C-1		6			
4	SB	67		273	6.067	0.067
	IBTA		5			
5	SBC	50		328	7.269	0.269
	C-1		5			
6	EXPOSURE	25		358	7.956	0.956
	S1		6			
7	PEB	65		429	9.533	0.533
	IBTA		5			
8	PEBC	50		484	10.756	0.756
	C-1		6			
9	DEV	110		600	13.333	0.333
	C-1		6			
10	HB	35		641	14.244	0.244
	C-1		6			
11	HBC	32		685	15.089	0.089
	CES		6			
12	CASSETTE	0		685	15.222	0.222
	0		0			
13	Vacant	0		685	0.000	0.000
	0		0			
14	Vacant	0		685	0.000	0.000
	0		0			
15	Vacant	0		685	0.000	0.000
	0		0			
16	Vacant	0		685	0.000	0.000
	0		0			
17	Vacant	0		685	0.000	0.000
	0		0			
18	Vacant	0		685	0.000	0.000
			0			

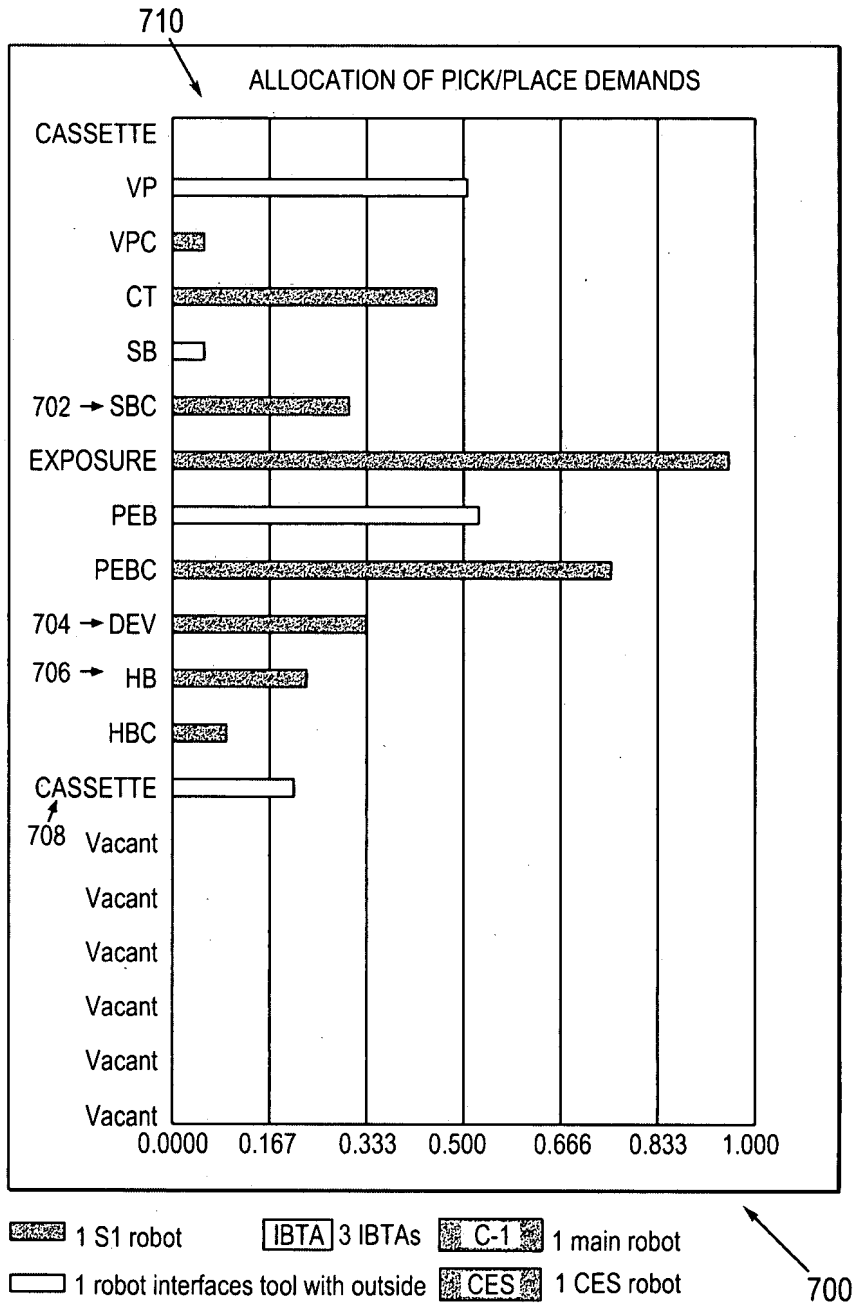
602
604
600
606
608
610



Vacant	0.000
Vacant	0.000
Vacant	0.000
Vacant	0.000
Vacant	0.000
Vacant	0.000
CASSETTE	0.222
HBC	0.089
HB	0.244
DEV	0.333
PEBC	0.756
PEB	0.533
EXPOSURE	0.956
SBC	0.289
SB	0.067
CT	0.444
VPC	0.067
VP	0.511
CASSETTE	0.000

Fig. 6

Process Step	Module type Transport type	Fraction of sending period
0	CASSETTE	0.000
	CES	
1	VP	0.511
	IBTA	
712→ 2	VPC	0.067
	C-1	
714→ 3	CT	4.444
	C-1	
4	SB	0.067
	IBTA	
716→ 5	SBC	0.269
	C-1	
6	EXPOSURE	0.956
	S1	
7	PEB	0.533
	IBTA	
718→ 8	PEBC	0.756
	C-1	
720→ 9	DEV	0.333
	C-1	
722→ 10	HB	0.244
	C-1	
11	HBC	0.089
	CES	
12	CASSETTE	0.222
	0	
13	Vacant	0.000
	0	
14	Vacant	0.000
	0	
15	Vacant	0.000
	0	
16	Vacant	0.000
	0	
17	Vacant	0.000
	0	
18	Vacant	0.000

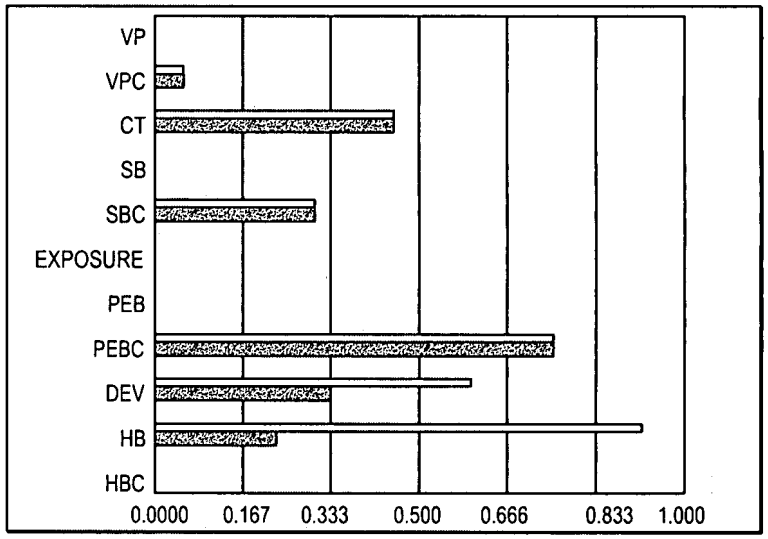


Vacant	0.000
Vacant	0.000
Vacant	0.000
Vacant	0.000
Vacant	0.000
Vacant	0.000
CASSETTE	0.222
HBC	0.089
HB	0.244
DEV	0.333
PEBC	0.756
PEB	0.533
EXPOSURE	0.956
SBC	0.289
SB	0.067
CT	0.444
VPC	0.067
VP	0.511
CASSETTE	0.000

Fig. 7

Table 1

Process Step (1)	Module type (2)	8 As-Is (3)	80 Target (4)	80+0 Gap (5)	9 Clue (6)	Actual Clue (6)
0	CASSETTE	0.000	0.000	0.000	0.000	0.000
1	VP	0.511	0.511	0.000	0.000	0.000
2	VPC	0.067	0.067	0.000	0.000	0.000
3	CT	0.444	0.444	0.000	0.000	0.000
4	SB	0.067	0.067	0.000	0.000	0.000
5	SBC	0.289	0.289	0.000	0.000	0.000
6	EXPOSURE	0.956	0.956	0.000	0.000	0.000
7	PEB	0.533	0.533	0.000	0.000	0.000
8	PEBC	0.756	0.756	0.000	0.000	0.000
9	DEV	0.333	0.333	0.267	0.267	12.000
10	HB	0.244	0.244	0.678	0.411	18.490
11	HBC	0.069	0.069	0.000	0.322	14.510
12	CASSETTE	0.222	0.222	0.000	0.000	0.000
13	Vacant	0.000	0.000	0.000	0.000	0.000
14	Vacant	0.000	0.000	0.000	0.000	0.000



Gap
0.000
0.000
0.000
0.000
0.000
0.000
0.000
0.000
0.267
0.678
0.000

Table 2 Matrix relating gaps to queues. See Eq (3) of text

1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0
1	1	1	1	1	1	0	0	0	0	0
1	1	1	1	1	1	1	0	0	0	0
1	1	1	1	1	1	1	1	0	0	0
1	1	1	1	1	1	1	1	1	0	0
1	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1

X

Que
0.000
0.000
0.000
0.000
0.000
0.000
0.000
0.000
0.267
0.411
-0.678

Table 3 Modified matrix to imposed constraints qi = 1=3,4,7 See Eq (4) Of text.

1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	0	0	1	1	0	0	0	0	0
0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	1	1	0	1	0	0	0
1	1	0	0	1	1	0	1	1	0	0
1	1	0	0	1	1	0	1	1	1	0
1	1	0	0	1	1	0	1	1	1	1

Que
0.000
0.000
0.000
0.000
0.000
0.000
0.000
0.000
0.267
0.411
-0.678

Table 4 Inverse of "constraint" matrix

1	0	0	0	0	0	0	0	0	0	0
-1	1	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0
0	-1	0	0	1	0	0	0	0	0	0
0	0	0	0	-1	1	0	0	0	0	0
0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	-1	0	1	0	0	0
0	0	0	0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	0	-1	1	0
0	0	0	0	0	0	0	0	0	-1	1

X

Gap
0.000
0.000
0.000
0.000
0.000
0.000
0.000
0.000
0.27
0.68
0.000

Fig. 8

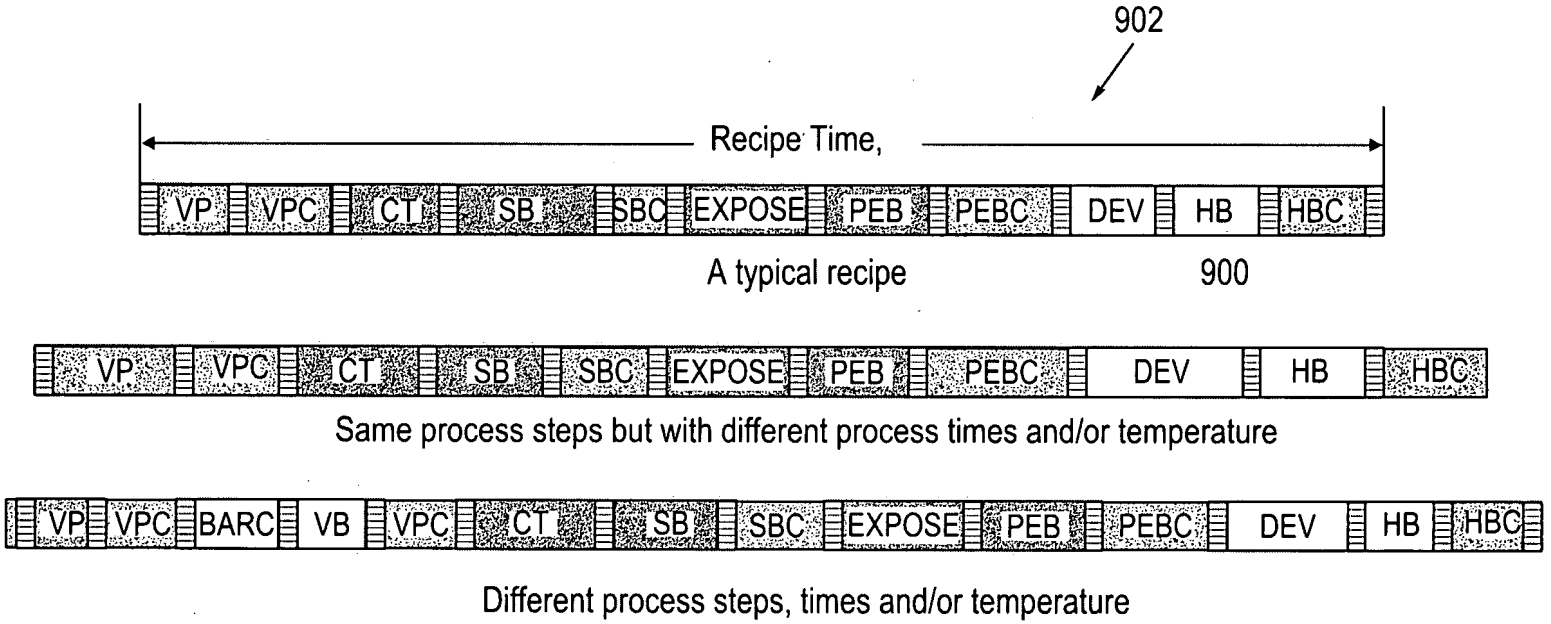

902
Recipe Time,
VP
VPC
CT
SB
SBC
EXPOSE
PEB
PEBC
DEV
HB
HBC
A typical recipe
900
VP
VPC
CT
SB
SBC
EXPOSE
PEB
PEBC
DEV
HB
HBC
Same process steps but with different process times and/or temperature
VP
VPC
BARC
VB
VPC
CT
SB
SBC
EXPOSE
PEB
PEBC
DEV
HB
HBC
Different process steps, times and/or temperature
Color legend:
Process critical, no delay allowed
Process somewhat critical, some delay allowed
Process not critical, delay allowed
Wafer transport

Fig. 9

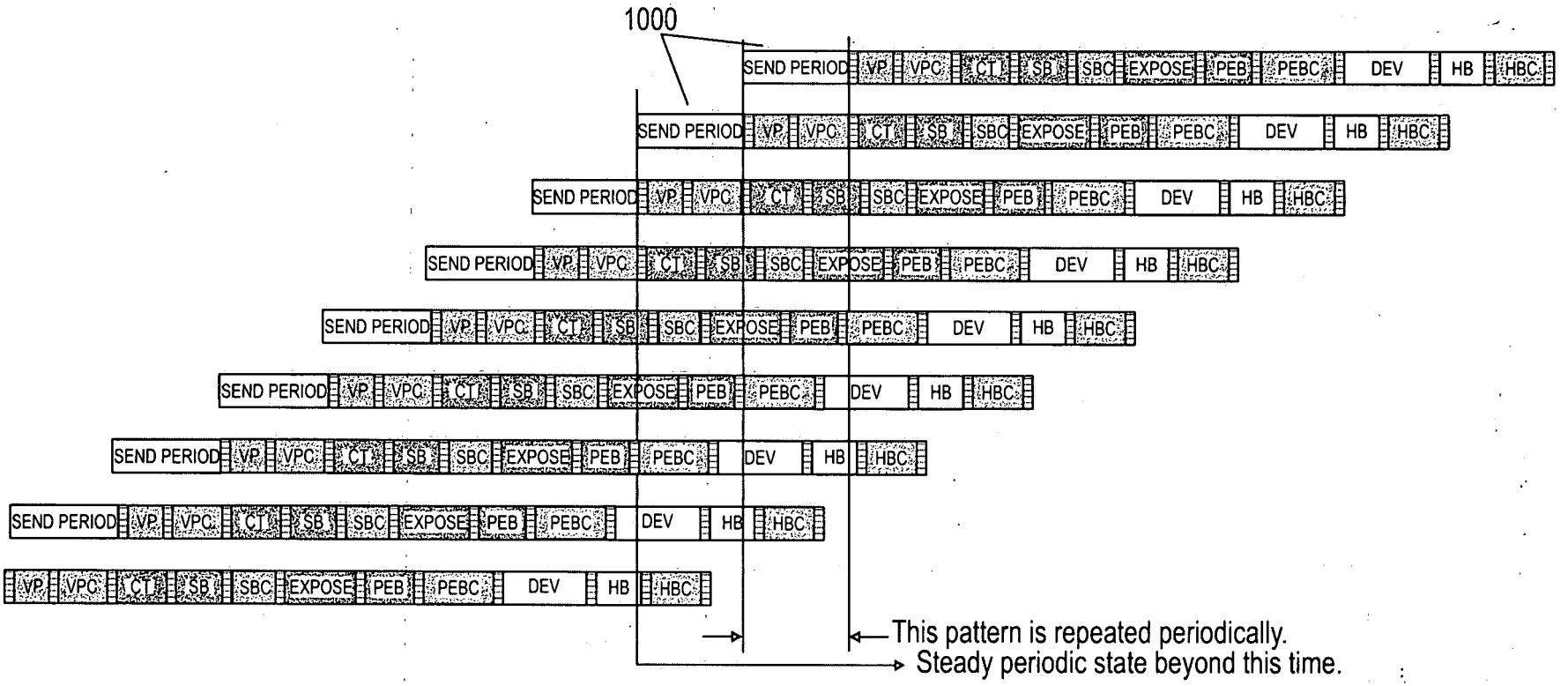

1000
SEND PERIOD
VP
VPC
CT
SB
SBC
EXPOSE
PEB
PEBC
DEV
HB
HBC
This pattern is repeated periodically.
Steady periodic state beyond this time.

Fig. 10

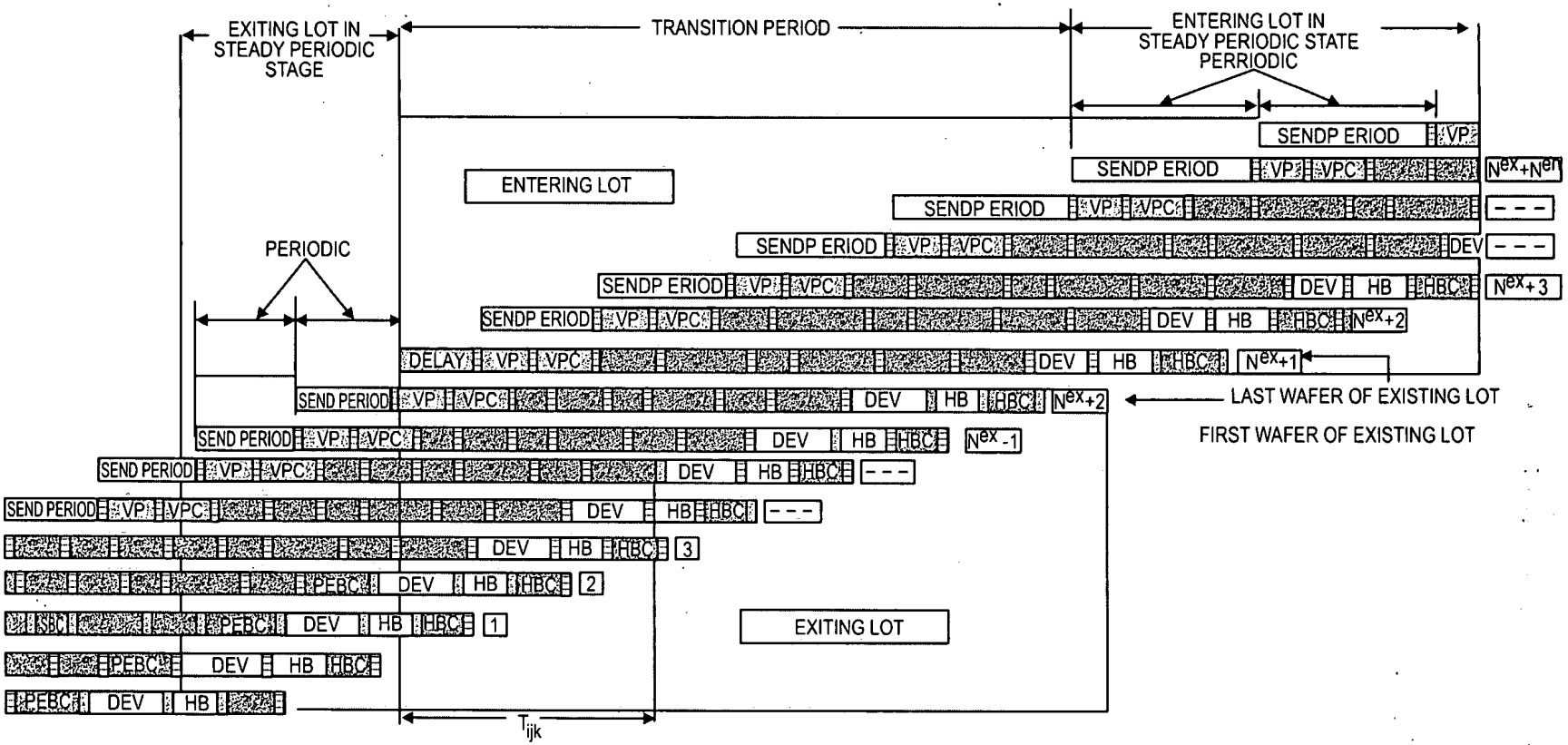

EXITING LOT IN STEADY PERIODIC STAGE
TRANSITION PERIOD
ENTERING LOT IN STEADY PERIODIC STATE PERRIODIC
ENTERING LOT
PERIODIC
EXITING LOT
LAST WAFER OF EXISTING LOT
FIRST WAFER OF EXISTING LOT
SENDP ERIOD
SEND PERIOD
DELAY
VP
VPC
DEV
HB
HBC
PEBC
SBC
$N^{ex}+N^{en}$
$N^{ex}+3$
$N^{ex}+2$
$N^{ex}+1$
$N^{ex}-1$
T_{ijk}

Fig. 11

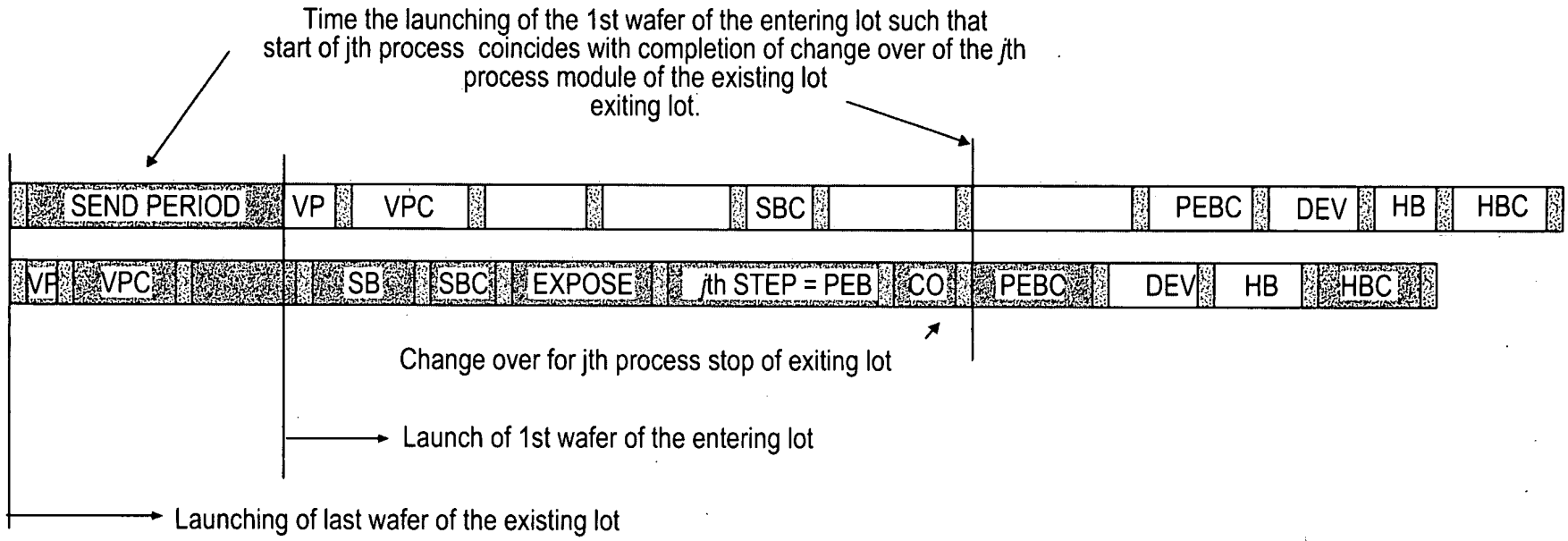

Time the launching of the 1st wafer of the entering lot such that start of jth process coincides with completion of change over of the jth process module of the existing lot exiting lot.
SEND PERIOD
VP
VPC
SBC
PEBC
DEV
HB
HBC
VP
VPC
SB
SBC
EXPOSE
jth STEP = PEB
CO
PEBC
DEV
HB
HBC
Change over for jth process stop of exiting lot
Launch of 1st wafer of the entering lot
Launching of last wafer of the existing lot

Fig. 12

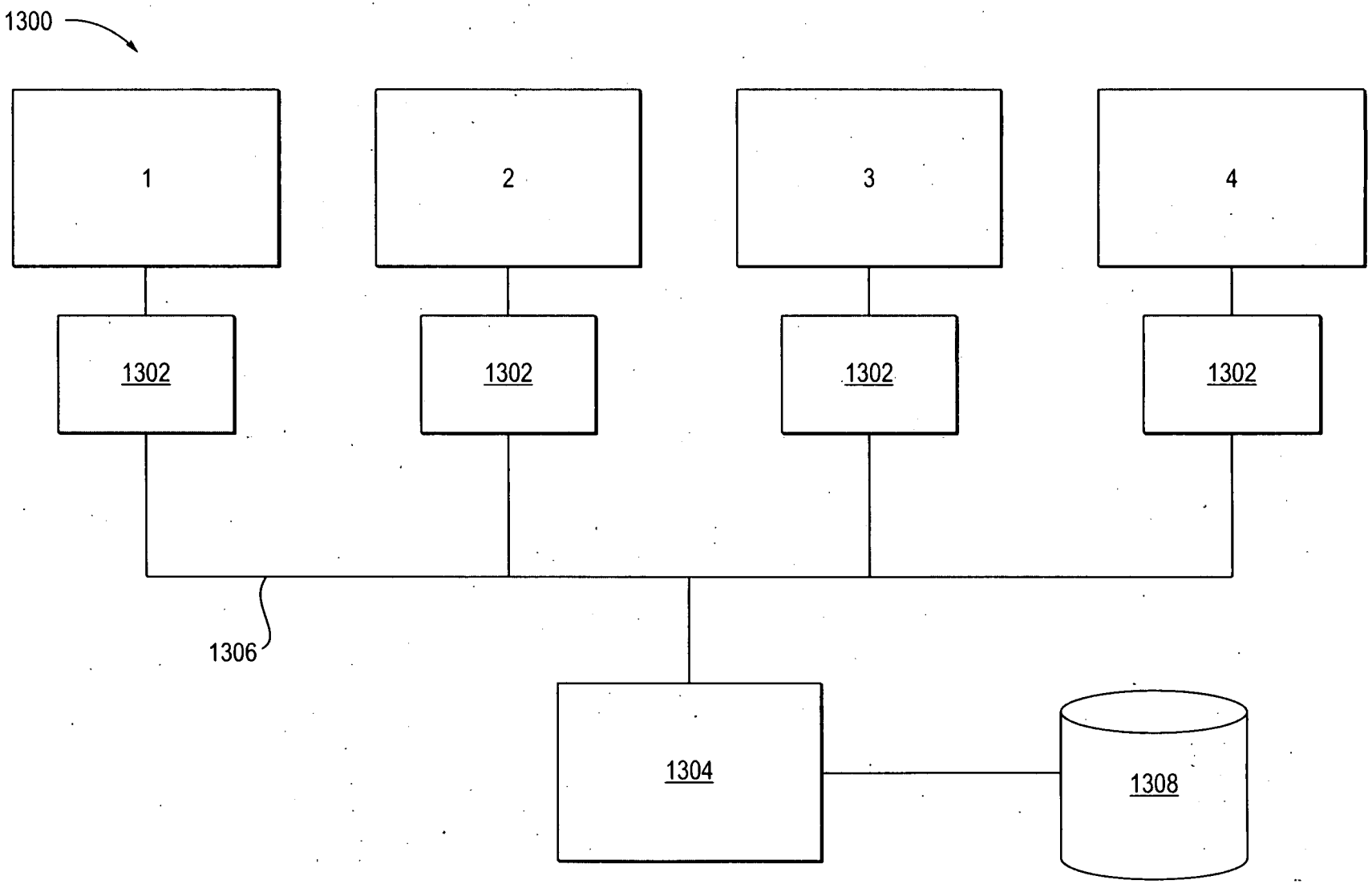


Fig. 13

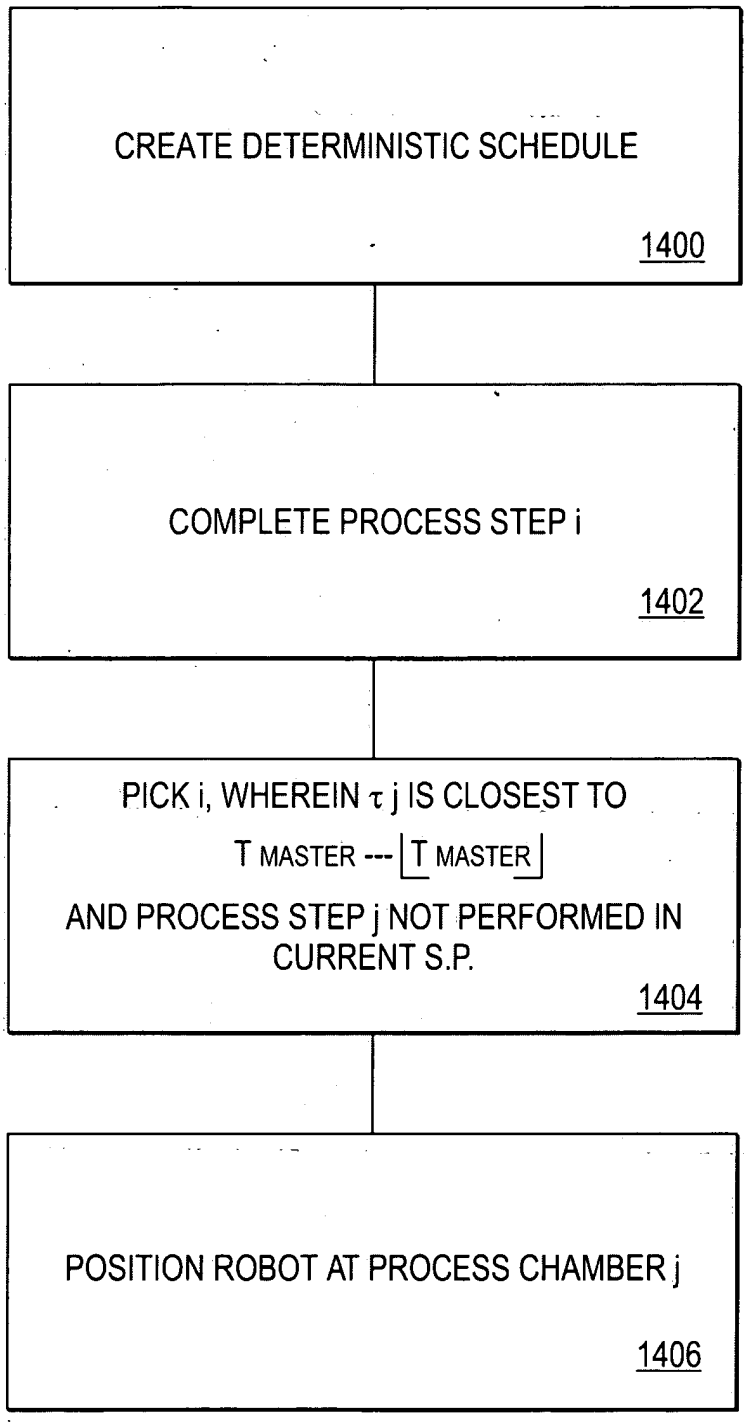

CREATE DETERMINISTIC SCHEDULE
1400
COMPLETE PROCESS STEP i
1402
PICK i, WHEREIN τ j IS CLOSEST TO
T MASTER --- ⌊T MASTER⌋
AND PROCESS STEP j NOT PERFORMED IN CURRENT S.P.
1404
POSITION ROBOT AT PROCESS CHAMBER j
1406

Fig. 14